Homework 6: Printed Circuit Board Layout Design

Due: Friday, February 24, at NOON

Team Code Name: Digital Real-Time Networked Kegerator **Group No. 4**

Team Member Completing This Homework: Dustin Poe

NOTE: This is the third in a series of four "design component" homework assignments, each of which is to be completed by one team member. The completed homework will count for 10% of the team member's individual grade. The report itself should be a minimum of five pages, **not** including the cover sheet, references, or any of the attachments (statistics report). **Electronically submit the ".MAX" PCB layout file along with the ".doc" version of this report zipped into one file.**

Evaluation:

Component/Criterion	Score	Multiplier	Points
Introduction & Layout Considerations	0 1 2 3 4 5 6 7 8 9 10	X 3	
Documentation for PCB Layout Design	0 1 2 3 4 5 6 7 8 9 10	X 5	
List of References	0 1 2 3 4 5 6 7 8 9 10	X 1	
Technical Writing Style	0 1 2 3 4 5 6 7 8 9 10	X 1	
		TOTAL	

Comments:

1.0 Introduction

The Digital Real Time Intelligent Networked Kegerator (DRINK) gives owners complete control of their existing beverage dispensing unit. The DRINK system provides control, monitoring and recording for beverages on a per user basis. This is accomplished by the core of the DRINK system, the control module. The control module was designed to meet the packaging requirements of the design constraints while minimizing conducted and radiated emissions.

2.0 PCB Layout Design Considerations

2.1 Packaging Requirements

The Printed Circuit Board layout for the control module was influenced by several factors. First, due the requirements of the packaging assembly, the board was limited to 115mm by 235mm. These dimensions are based the width and height of the currency acceptor in which the PCB will mount. To facilitate mounting screw holes have been placed at the four corners.

2.2 PCB Partitioning

The PCB was partitioned into sections to ease routing and to allow for simpler interfaces. One PCB section is the common beverage interface that's located at the bottom edge of the board. The PCB and schematic were designed so that a maximum of 4 beverages can be recorded at one time. The signals were laid out so that each connector has all the necessary signals to interface to one beverage. These pins include a 12V Power Signal, a 5 Power Signal, a 12 Volt Return, a 5V Return, a 5V beverage connected signal and a 5V pulse signal to indicate flow. This connector is one of the many custom footprints created in this design.

Next to the beverage interface is another partition the temperature and compressor interface. This interface includes the connectors for the temperature sensors and the compressor relay. This connector was chosen because of its high current rating and small package.

Another layout section is the Rabbit Core. This section is the heart of the system and performs most of the necessary logic for the DRINK system. The Rabbit receptacles were custom made because of its rare 2mm pitch spacing. Every Rabbit signal was brought out to a

header for troubleshooting and debugging purposes. A backup battery was provided for the Rabbit to ensure that the recorded data would not be lost in case of a no power condition. Included also in this section is a Audio Transducer that will be used to indicate a successful user identification. Finally, for troubleshooting reasons a reset switch was included on the PCB layout. These three parts all required custom footprints.

The next layout section is the 3.3V and 5V Power Circuits. This section consists of two switching DC to DC converters that create 5V and 3.3V from 12V. Each supply is capable of generating up to an amp of current. Special Tantalum capacitors were required in this section because of their low Equivalent Series Resistance. These capacitors required custom footprints as well. Decoupling capacitors were mounted on the back side of the board to supply instantaneous current. They were mounted on the backside in order to place them as close to the power supplies as possible [1].

The Power section consists of only of a 12 VDC power receptacle. Similar to most components in this layout it was also a custom footprint. This connector will mate up with an AC in line transformer which creates the 12V. The center pin of this power receptacle is 12V while the other shell is ground. It is in this section that the separate grounds for Digital and Analog are tied together. The two grounds are tied together at one point to reduce common mode noise. Please note that in the schematic separate nets were created for Digital and the analog ground. This allowed for easier routing. These two nets are tied together at a point. At this point however is where a Design Rule Check Flags an error see Appendix A.

Another section of the layout is the Serial Interface. This section includes: the RS-232 translators, the LCD headers, the RFID chip, the currency acceptor headers, and the Rotary Pulse Generator header. The RFID and the LCD headers required custom footprints, but all other were standard. The Maxim RS-232 Translator required decoupling caps. These caps were mounted as close to the translator as possible to minimize interference.

The final section in this layout is the biometric and future development. In this section an optional biometric thumb print reader can be connected to the micro. The header and its signals are designed so that other serial devices may also be connected. Finally, a PLD brought out to headers is included in case other I]/O is needed. All of these components had standard footprints.

2.3 Signal Routing

To facilitate routing, Power and Ground traces were placed first. All traces were made to have non acute angles to reduce interference. On the bottom edge of the board near the dc to dc converter a 12V power trace was laid having a dimension of 50 mil. The maximum current this trace will have is 3 Amps. This is because the DC to DC converter along with the currency acceptor will have a peak current of 3 Amps. According to the trace width calculator a minimum trace size of 24 mils would be acceptable [3]. However a 50 mil was chosen because of the PCB recommendations of Module 2 [5]. Wherever possible Power and Ground traces were ran directly on top of each other. This was a recommendation from a Motorola App Note [2]. Another Power and Ground rail were placed along the beverage interface. This trace was located between the through hole pin and the signal pin of the beverage connector. This will provide easy traces for the Beverage Connectors, since each connector requires 12 V for its solenoids. The trace width for this was 60 mils because a potential 4 Amps is possible if all for solenoids are exerted at once. Once the 12 Volt power and ground was in place, the Digital Ground came next. All Digital Ground traces were routed to the top and the left of the board. This separated the noisy digital ground from the analog ground and prevented noise from coupling onto analog. The Digital and Analog Ground were then tied together at a single point near the DC Power Receptacle. The DC to DC switching power supplies each had two ground supplies. The grounds were separated in order to reduce conducted emissions. Once the digital ground was in place the 5V and the 3.3 Volt traces were created. The 5V trace was located on top directly above the digital ground. This was done again to help reduce noise. In routing the digital signals several different techniques were used. Often bottom traces were ran vertically while top traces were ran horizontally. This greatly simplified the routing. Another method that simplified the routing is was symmetrical placement of components. Each beverage had the same components, by placing the components the same the traces could be made to look the same as well. Once all traces were placed, the partitions were divided up so that the silk screen objects could be placed to properly identify them. In addition silk screen text was placed near all the headers to indicate what they interfaced to.

3.0 Summary

The Digital Real Time Networked Kegerator provides total beverage management. Its control module was created to maximize space without sacrificing functionality. Much care was taken in order to reduce the Electromagnetic interference. Some of the methods applied include: Tying ground together at a single point, routing power and ground directly on top of each other, and preventing acute angle traces.

Be sure to read Motorola Application Note AN1259 (posted on course web site) before you begin your PCB layout.

List of References

[1] Linear Technology, "LTC1265/LTC1265-3.3/LTC1265-5 Data Sheet," [Online Document], 1995, [cited 2006 Feb 23] Available HTTP: **http://www.linear.com/pc/downloadDocument.do?navId=H0,C1,C1003,C1042,C1032,C1064,P1162,D1159**

[2] "System Design and Layout Techniques for Noise Reduction in MCU-Based Systems" Motorola Semiconductor Application note AN1259/D [Online Document] 1995, [cited 2006 Feb 23], Available HTTP: **http://shay.ecn.purdue.edu/~dsml/ece477/Homework/Spr2006/AN1259.pdf**

[3] The Circuit Calculator.com Blog "PCB Trace Width Calculator [Online Document] 2006 Jan 31, [cited 2006 Feb 23] Available HTTP: **http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator/**

[4**]** Rabbit Semiconductor "PC Board Layout Suggestions to Reduce EMI and RF Emissions with the Rabbit 3000® Microprocessor" **http://www.rabbitsemiconductor.com/documentation/docs/refs/TN221/tn221.htm**

[5] Professor D.G. Meyer "Module 2: Digital System Design Considerations and PCB Layout Basics" [Online Document] 2006 [cited 2006 Feg 23] Available HTTP: **http://shay.ecn.purdue.edu/~dsml/ece477/Notes/PDF/4-Mod2.pdf**

IMPORTANT: Use standard IEEE format for references, and CITE ALL REFERENCES listed in the body of your report. Provide "live" links to all data sheets utilized.

Appendix A: Routing Statistics Report

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*                                    *
*  STATISTICS REPORT                 *
*                                    *
* R:\EE477\LAYOUT\FEB25-9AMTEST1.MAX  *
*  Sat Feb 25 11:12:57 2006          *
*                                    *
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STATISTIC	ENABLED	TOTAL
Board Area	42.8	42.8
Equivalent IC's	39.5	39.5
Sq. inches per IC	1.09	1.09
# of pins	592	592
Layers	4	28
Design Rule Errors	21	21
Time Used	38:35	38:35
% Placed	100.00%	100.00%
Placed	116	116
Off board	0	0
Unplaced	0	0
Clustered	0	0
Routed	647	647
% Routed	99.23%	99.23%
Unrouted	0	0
% Unrouted	0.00%	0.00%
Partials	5	5
% Partials	0.77%	0.77%
Vias	178	178
Test Points	0	0
Vias per Conn	0.27	0.27
Segments	4780	4780
Connections	652	652
Nets	141	141
Components	116	116
Footprints	202	202
Padstacks	70	70
Obstacles	603	603
Theoretical Dist	451.8	451.8
Routed Dist	404.6	404.6
Unrouted Dist	20.2	20.2